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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

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of

1

Complete if Known

Application Number	10/627,218
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Filing Date	July 25, 2003
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First Named Inventor	Yeo, et al.
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Art Unit	2831
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Examiner Name

Ha

Attorney Docket Number

TSM03-0556

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

[illegible]

**Examiner
Signature**

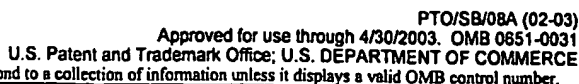
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U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
NH	1	US-4,314,269	02-02-1982	Fujiki	
	2	US-4,631,803	12-30-1986	Hunter, et al.	
	3	US-4,946,799	08-07-1990	Blake, et al.	
	4	US-5,447,884	09-05-1995	Fahey, et al.	
	5	US-5,461,250	10-24-1995	Burghartz, et al.	
	6	US-5,534,713	07-09-1996	Ismail, et al.	
	7	US-5,629,544	05-13-1997	Voldman, et al.	
	8	US-5,714,777	02-03-1998	Ismail, et al.	
	9	US-5,763,315	06-09-1998	Benedict, et al.	
	10	US-5,811,857	09-22-1998	Assaderaghi, et al.	
	11	US-6,008,095	12-28-1999	Gardner, et al.	
	12	US-6,015,993	01-18-2000	Voldman, et al.	
	13	US-6,046,487	04-04-2000	Benedict, et al.	
	14	US-6,059,895	05-09-2000	Chu, et al.	
	15	US-6,222,234 B1	04-24-2001	Imai	
	16	US-6,232,163 B1	05-15-2001	Voldman, et al.	
	17	US-6,291,321 B1	09-18-2001	Fitzgerald	
	18	US-6,294,834 B1	09-25-2001	Yeh, et al.	
	19	US-6,387,739 B1	05-14-2002	Smith, III	
	NH	20	US-2002/0076899 A1	06-20-2002	Skotnicki, et al.
21		US-6,413,802 B1	07-02-2002	Hu, et al.	
	22	US-6,414,355 B1	07-02-2002	An, et al.	

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/627,218
				Filing Date	July 25, 2003
				First Named Inventor	Yeo, <i>et al.</i>
				Art Unit	2831
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0556
Sheet	2	of	5		

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Examiner Signature		Date Considered	11/3/04
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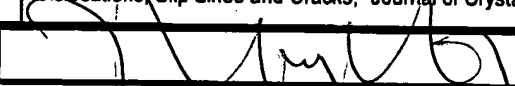
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Application Number	10/627,218
		Filing Date	July 25, 2003
		First Named Inventor	Yeo, <i>et al.</i>
		Group Art Unit	2831
		Examiner Name	TBD
		Attorney Docket Number	TSM03-0556
Sheet	3	of	5

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cita. No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	²
014	32	ISMAIL, K., <i>et al.</i> , "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," <i>Applied Physics Letters</i> , Vol. 63, No. 5, (August 2, 1993), pp. 660-662.	
	33	NAYAK, D.K., <i>et al.</i> , "Enhancement-Mode Quantum-Well Ge _x Si _{1-x} PMOS," <i>IEEE Electron Device Letters</i> , Vol. 12, No. 4, (April 1991), pp. 154-156.	
	34	GAMIZ, F., <i>et al.</i> , "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," <i>Applied Physics Letters</i> , Vol. 80, No. 22, (June 3, 2002), pp. 4160-4162.	
	35	GAMIZ, F., <i>et al.</i> , "Electron Transport in Strained Si Inversion Layers Grown on SiGe-on-Insulator Substrates," <i>Journal of Applied Physics</i> , Vol. 92, No. 1, (July 1, 2002), pp. 288-295.	
	36	MIZUNO, T., <i>et al.</i> , "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," <i>IEEE Transactions on Electron Devices</i> , Vol. 49, No. 1, (January 2002), pp. 7-14.	
	37	TEZUKA, T., <i>et al.</i> , "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique," <i>Symposium On VLSI Technology Digest of Technical Papers</i> , (2002), pp. 96-97.	
	38	JURCZAK, M., <i>et al.</i> , "Silicon-on-Nothing (SON) - an Innovative Process for Advanced CMOS," <i>IEEE Transactions on Electron Devices</i> , Vol. 47, No. 11, (November 2000), pp. 2179-2187.	
	39	JURCZAK, M., <i>et al.</i> , "SON (Silicon on Nothing) - A NEW DEVICE ARCHITECTURE FOR THE ULSI ERA," <i>Symposium on VLSI Technology Digest of Technical Papers</i> , (1999), pp. 29-30.	
	40	MAITI, C.K., <i>et al.</i> , "Film Growth and Material Parameters," <i>Application of Silicon-Germanium Heterostructure</i> , Institute of Physics Publishing, Ch. 2 (2001) pp. 32-42.	
	41	TIWARI, S., <i>et al.</i> , "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," <i>International Electron Device Meeting</i> , (1997), pp.939-941.	
	42	OOTSUKA, F., <i>et al.</i> , "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," <i>International Electron Device Meeting</i> , (2000), pp. 575-578.	
	43	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers - I. Misfit Dislocations," <i>Journal of Crystal Growth</i> , Vol. 27, (1974), pp. 118-125.	
014	44	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers - II. Dislocation Pile-Ups, Threading Dislocations, Slip Lines and Cracks," <i>Journal of Crystal Growth</i> , Vol. 29, (1975), pp. 273-280.	
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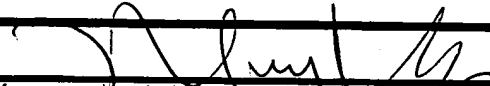
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		Filing Date	July 25, 2003
		First Named Inventor	Yeo, <i>et al.</i>
		Group Art Unit	2831
		Examiner Name	TBD
		Attorney Docket Number	TSM03-0556
Sheet	4	of	5

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
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20H	45	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers – III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.	
	46	SCHÜPPEN, A., <i>et al.</i> , "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, (1995), pp. 298-305.	
	47	MATTHEWS, J.W., "Defects Associated with the Accommodation of Misfit Between Crystals," J. Vac. Sci. Technol., Vol. 12, No. 1 (Jan./Feb. 1975), pp. 126-133.	
	48	HUANG, X., <i>et al.</i> , "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pp. 880-886.	
	49	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 121-131.	
	50	SHIMIZU, A., <i>et al.</i> , "Local Mechanical Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEDM 2001, pp. 433-436.	
	51	WONG, H.-S.P., "Beyond the Conventional Transistor," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 133-167.	
	52	YANG, F.L., <i>et al.</i> , "25 nm CMOS Omega FETs," IEDM 2002, pp. 255-258.	
	53	YANG, F.L., <i>et al.</i> , "35nm CMOS FinFETs," 2002 Symposium on VLSI Technology Digest of Technical Papers, 2002, pp. 104-105.	
	54	THOMPSON, S., <i>et al.</i> , "A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm^2 SRAM Cell," IEDM, pp. 61-64.	
	55	WELSER, J., <i>et al.</i> , "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM 1992, pp. 1000-1002.	
	56	BLAAUW, D., <i>et al.</i> , "Gate Oxide and Subthreshold Leakage Characterization, Analysis and Optimization," date unknown.	
20H	57	"Future Gate Stack," International Sematech, 2001 Annual Report.	
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